3. The method of claim 2, wherein said determining the status of the re-routing bridge in the bus interface comprises checking a status of a bridge-enable bit in a control register.

A1

8. Apparatus comprising:

a processor core including

a memory including a local data memory and a local instruction memory,

a first port coupled to the local data memory, and a second port coupled to the local data memory and the local instruction memory; and

a bus interface including

A2

a first bus coupled to the first port,

a second bus coupled to the second port,

a bridge between the first bus and the second bus, and

a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be re-routed into the second port.

15. An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause:

A3

a machine to route a memory access from a processor core back into the processor core through a bus interface coupled to the processor core.

22. A system comprising:

a processor comprising

a local memory including a local data memory and a local instruction memory,

a first port coupled to the local data memory, and

a second port coupled to the local data memory and the local instruction memory; and

a bus interface including

a first bus coupled to the first port,

a second bus coupled to the second port,

a bridge between the first bus and the second bus, and

a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be re-routed into the second port; and

a USB (Universal Serial Bus) interface.

23. The system of claim 22, wherein the local memory has an address space, and further comprises a bus control unit operative to switch the multiplexer to the bridge in response to a bridge-enable flag being set and an address of a memory

location associated with a memory access from the processor core falls within the local memory address space.

Please add new claims 29-32 as follows.

29. The apparatus of claim 8, wherein the memory is a local memory.

30. Apparatus comprising:

a bus interface; and

a processor connected to the bus interface, the processor being operative to reroute a memory access from the processor back into the processor through the bus interface.

31. The apparatus of claim 30, wherein the processor includes a local instruction memory.

32. The apparatus of claim 31 wherein the processor is operative to access the local instruction memory by rerouting a memory access through the bus interface.